CLAIMS

1. A semiconductor device comprising a protruding semiconductor region formed on a substrate, a protruding source/drain region sandwiching the semiconductor region and a gate electrode formed at least on lateral sides of the semiconductor region via an insulating film,

wherein the source/drain region has a slope in which at least the largest width is larger than a width of the semiconductor region and width continuously increases from the uppermost side to the substrate side in the source/drain region, and a silicide film is formed on the surface of the slope.

2. A semiconductor device comprising a plurality of protruding semiconductor regions formed on a substrate, a plurality of source/drain regions sandwiching the semiconductor regions and a gate electrode formed at least on lateral sides of the semiconductor regions via an insulating film,

wherein the plurality of semiconductor regions are aligned in a direction perpendicular to a channel current flow and in parallel with each other, and the gate electrode strides over the plurality of semiconductor regions and extends in a direction perpendicular to the channel current flow,

wherein the source/drain regions have slopes in which at least the largest width is larger than a width of the semiconductor region and width continuously increases from the uppermost side to the substrate side in the source/drain regions, and a silicide film is formed on the surface of the slopes .

3. A semiconductor device comprising a plurality of protruding semiconductor regions formed on a substrate, a paired protruding source/drain region which is common to the plurality of semiconductor regions and sandwiches the plurality of semiconductor regions, and a gate electrode formed at least on lateral sides of the plurality of semiconductor regions via an insulating film,

wherein the plurality of semiconductor regions are aligned in a direction perpendicular to a channel current flow and in parallel with each other, and the gate electrode strides over the plurality of semiconductor regions and extends in a direction perpendicular to the channel current flow,

wherein the source/drain region has a concavity and convexity portion in which a cross-sectional area continuously increases from the uppermost side to the substrate side, and a silicide film is formed on the surface of the concavity and convexity portion.

4. The semiconductor device as claimed in Claim 3, wherein the concavity and convexity portion are formed in the direction of alignment of the plurality of semiconductor regions at the same regular intervals as the plurality of semiconductor regions such that the semiconductor regions are in parallel with the concavity and convexity portion.

5. The semiconductor device as claimed in any of Claims 1 to 4, wherein the uppermost side of the source/drain region(s) is parallel with a plane of the substrate and a silicide film is formed on the uppermost side.

6. The semiconductor device as claimed in Claim 1 or 2, wherein the whole of the source/drain region(s) is composed from the slope(s) having a silicide film on its surface.

7. The semiconductor device as claimed in Claim 1 or 2, wherein a width of the slope(s) in the source/drain region(s) increases from the uppermost side to the substrate side in a constant rate.

8. The semiconductor device as claimed in Claim 3, wherein the cross-sectional area of the concavity and convexity portion increases from the uppermost side to the substrate side in a constant rate.

9. A process for manufacturing a semiconductor device comprising a field effect transistor having a protruding semiconductor region in whose lateral

sides a channel is formed, comprising

(a) forming a protruding source/drain region sandwiching the protruding semiconductor region with a gate electrode by selective epitaxial growth to make a slope in which a width of the source/drain region is larger than a width of the semiconductor region and continuously increases from the uppermost side to the substrate side in the source/drain region, and (b) forming a silicide film on the surface of the slope.

10. A process for manufacturing a semiconductor device comprising a field effect transistor having a plurality of protruding semiconductor regions in whose lateral sides a channel is formed, comprising

(a) forming a gate electrode striding over the plurality of protruding semiconductor regions, then forming a plurality of protruding source/drain regions sandwiching the plurality of semiconductor regions by selective epitaxial growth to make slopes in which a width of the source/drain regions is larger than a width of the semiconductor regions and continuously increases from the uppermost side to the substrate side in the source/drain regions, and (b) forming a silicide film on the surface of the slopes.

11. A process for manufacturing a semiconductor device comprising a field effect transistor having a plurality of protruding semiconductor regions in whose lateral sides a channel is formed, comprising

(a) forming a gate electrode striding over the plurality of protruding semiconductor regions, then forming a plurality of protruding source/drain regions sandwiching the plurality of semiconductor regions by selective epitaxial growth until adjacent source/drain regions come into contact each other to make a concavity and convexity portion where a cross-sectional area of the source/drain regions continuously increase from the uppermost side to the substrate side in the source/drain regions during the selective epitaxial growth,

and (b) forming a silicide film on the surface of the concavity and convexity portion.

12. The process for manufacturing a semiconductor device as claimed in Claim 9 or 10, wherein the slope(s) is formed by selective epitaxial growth in substantially up to eight crystal faces in a cross section which is in parallel with the width direction and with the direction from the uppermost side to the substrate side of the source/drain region(s) and intersects with the uppermost side.

13. The process for manufacturing a semiconductor device as claimed in Claim 11, wherein the concavity and convexity portion are formed by selective epitaxial growth in substantially up to eight crystal faces in a cross section which is in parallel with the width direction and with the direction from the uppermost side to the substrate side of the source/drain regions and intersects with the uppermost side.

14. The process for manufacturing a semiconductor device as claimed in Claim 9 or 10, wherein the slope(s) is formed by selective epitaxial growth as a substantially curve in a cross section which is in parallel with the width direction and with the direction from the uppermost side to the substrate side of the source/drain region(s) and intersects with the uppermost side.

15. The process for manufacturing a semiconductor device as claimed in Claim 11, wherein the concavity and convexity portion are formed by selective epitaxial growth as a substantially curve in a cross section which is in parallel with the width direction and with the direction from the uppermost side to the substrate side of the source/drain regions and intersects with the uppermost side.

16. A process for manufacturing a semiconductor device comprising a field effect transistor having a protruding semiconductor region in whose lateral

sides a channel is formed, comprising,

(a) forming a gate electrode on the protruding semiconductor region and then etching a protruding source/drain region sandwiching the semiconductor region and having a larger width than the width of the semiconductor region, to make a slope in which a width of the source/drain region is larger than a width of the semiconductor region and continuously increases from the uppermost side to the substrate side in the source/drain region, and (b) forming a silicide film on the surface of the slope.

17. A process for manufacturing a semiconductor device comprising a field effect transistor having a plurality of protruding semiconductor regions in whose lateral sides a channel is formed, comprising,

(a) forming a gate electrode striding over the plurality of protruding semiconductor regions, forming a paired protruding source/drain region sandwiching the plurality of semiconductor regions, and then forming a mask film having a plurality of openings alternately with the plurality of semiconductor regions along the alignment direction of the semiconductor regions on the source/drain region, (b) conducting etching using the mask film to make the paired source/drain region into a plurality of source/drain regions mutually separated sandwiching the plurality of semiconductor regions and during the etching, making slopes in which a width of the source/drain regions is larger than a width of the semiconductor regions and continuously increases from the uppermost side to the substrate side in the source/drain regions, and (c) forming a silicide film on the slopes.

18. A process for manufacturing a semiconductor device comprising a field effect transistor having a plurality of protruding semiconductor regions in whose lateral sides a channel is formed, comprising,

(a) forming a gate electrode striding over the plurality of protruding

semiconductor regions, forming a paired protruding source/drain region sandwiching the plurality of semiconductor regions, and then forming a mask film having a plurality of openings alternately with the plurality of semiconductor regions along the alignment direction of the semiconductor regions on the source/drain region, (b) conducting etching using the mask film to make a concavity and convexity portion in which cross-sectional area continuously increases from the uppermost side to the substrate side in the source/drain region, and (c) forming a silicide film on the concavity and convexity portion.

19. The process for manufacturing a semiconductor device as claimed in any of Claims 16 to 18, wherein the etching is wet etching.

20. The semiconductor device as claimed in any of Claims 1 to 8, wherein the substrate is an insulating film layer, on which the protruding semiconductor region(s) and the protruding source/drain region(s) are formed.

21. The semiconductor device as claimed in any of Claims 1 to 8, wherein the substrate is an interlayer insulating film, and

the protruding semiconductor region(s) and the protruding source/drain region(s) are parts of the semiconductor layer formed under the interlayer insulating film, which penetrates the interlayer insulating film and protrudes above the interlayer insulating film.

22. The semiconductor device as claimed in any of Claims 1 to 8, 20 and 21, further comprising a planar type field effect transistor having a semiconductor region on whose upper surface a main channel is formed, and an elevated source/drain region.